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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,788	07/21/2003	Leonard Forbes	1303.109US1	6087

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,788	FORBES ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *54-65* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/12/04, 5/6/05,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the election on 9 December 2005. Claims 1-65 are pending.

Election/Restrictions

Applicant's election without traverse of group I, claims 1-53 in the reply filed on 9 December 2005 is acknowledged.

Claims 54-65 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9 December 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Beiver, Celeste "Secrets of 'strained silicon' revealed" *New Scientist* (17 December 2003).

Referring to claim 1, Beiver discloses a method for forming a wafer where a predetermined contour is formed in one of a semiconductor membrane and a substrate wafer; and bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane (carved trenches).

Referring to claim 2, Beiver discloses wherein the predetermined contour is straightened when the semiconductor membrane is bonded to the substrate wafer (carved trenches).

Referring to claim 3, Beiver discloses the semiconductor membrane is bonded to the substrate wafer before the predetermined contour is straightened (carved trenches).

Referring to claim 11, Beiver discloses the semiconductor membrane includes silicon (carved trenches).

Referring to claim 16, Beiver discloses flexing a substrate wafer into a flexed position; bonding a portion of the substrate wafer to a semiconductor layer when the substrate wafer is in the flexed position; and relaxing the substrate wafer to induce a predetermined strain in the semiconductor layer (carved trenches).

Claims 22, 26-28 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Belford (6,514,836).

Referring to claim 22, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33).

Referring to claim 26, Belford discloses bonding the upon bonding the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate (204) (col. 3, lines 16-33).

Referring to claim 27, Belford discloses the semiconductor membrane includes an ultra-thin semiconductor layer (col. 3, lines 16-33).

Referring to claim 28, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33 & 63-67).

Referring to claim 43, Belford discloses a method for forming a wafer including forming a concave surface in a crystalline wafer; bonding the concave surface of the crystalline wafer to a substrate wafer to induce a strain in the crystalline wafer; and

polishing the bonded crystalline wafer to thin the crystalline wafer and control the induced strain (Fig. 2; col. 3, lines 6-32).

Claims 31 33, 35-38 and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Doyle et al. (6,228,694).

Referring to claim 31, Doyle et al. disclose a method for forming a wafer where voids (56) are formed in a substrate wafer (50) to provide the substrate wafer with a desired flexibility; flexing the substrate wafer into a flexed position; bonding a portion of the substrate wafer to a semiconductor membrane when the substrate wafer is in the flexed position; and relaxing the substrate wafer to induce a predetermined strain in the semiconductor membrane (Fig. 5-7; col. 4, lines 40-54).

Referring to claim 33, Doyle et al. disclose wherein forming voids in a substrate wafer includes forming a predetermined arrangement of voids using a surface transformation process (col. 3, lines 54-63).

Referring to claim 35, Doyle et al. discloses forming voids in a substrate wafer includes forming holes in a substrate wafer having a well-defined melting temperature, and annealing the substrate wafer at a temperature that is close to and below the well-defined melting temperature (col. 4, lines 23-39).

Referring to claim 36, Doyle et al. disclose forming voids in a substrate wafer includes forming spherical voids using a surface transformation process, each of the spherical voids being a predetermined size and being positioned at a predetermined location (col. 4, lines 1-11).

Referring to claim 37, Doyle et al. disclose forming voids in a substrate wafer includes forming pipe-shaped voids using a surface transformation process, each of the pipe-shaped voids being a predetermined size and being positioned at a predetermined location (col. 4, lines 1-11).

Referring to claim 38, Doyle et al. disclose forming voids in a substrate wafer includes forming plate-shaped voids using a surface transformation process, each of the plate- shaped voids being a predetermined size and being positioned at a predetermined location (col. 3, line 64 thru col. 4, line 39).

Referring to claim 44, Doyle et al. disclose a method of forming a transistor where forming a strained semiconductor layer includes: forming a predetermined contour in one of a semiconductor layer and a substrate wafer; and bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer; forming a gate separated from the strained semiconductor layer by a gate insulator; and forming first and second diffusion regions separated by a channel region, the strained semiconductor layer including the first and second diffusion region and the channel region (Fig. 2A & 2B; col. 3, lines 27-43).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7, 9, 10, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biever in view of Belford.

Biever disclose the subject matter claimed above expect performing a bond cut process.

Referring to claims 4 and 9, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33 & 63-67).

Since Biever and Belford are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Belford would have been recognized in the pertinent art of Biever. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Biever by performing a bond cut process as taught by Belford to reduce the short channel effects (col. 1, lines 45-63).

Referring to claims 5 and 21, Belford discloses bonding the upon bonding the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate (204) (col. 3, lines 16-33).

Referring to claim 6, Belford discloses forming a predetermined contour in one of a semiconductor membrane and a substrate wafer includes applying a pressure to flex the substrate wafer to have a predetermined strain; and bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane includes: bonding a periphery of the membrane to a periphery of the substrate wafer; and removing the pressure to relax the substrate wafer and transfer strain from the substrate wafer to the semiconductor membrane (Fig. 2; col. 3, lines 18-33).

Referring to claims 7 and 10, Belford discloses applying a pressure to flex the substrate wafer to have a predetermined strain includes applying a pressure to a substrate wafer having a thickness sufficiently small such that the substrate wafer is flexible (col. 3, lines 6-32).

Referring to claims 13 and 17, Belford discloses the semiconductor membrane includes an ultra-thin semiconductor layer (col. 3, lines 16-33).

Referring to claim 14, Belford discloses the semiconductor membrane is between approximately 10 microns (col. 3. lines 25-29).

Claims 8, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biever in view of Doyle et al.

Biever discloses the subject matter claimed above expect forming voids in the substrate.

Referring to claim 8, Doyle et al. disclose a method for forming a wafer where voids (56) are formed in a substrate wafer (50) to provide the substrate wafer with a desired flexibility; flexing the substrate wafer into a flexed position; bonding a portion of the substrate wafer to a semiconductor membrane when the substrate wafer is in the flexed position; and relaxing the substrate wafer to induce a predetermined strain in the semiconductor membrane (Fig. 5-7; col. 4, lines 40-54).

Since Biever and Doyle et al. are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Doyle et al. would have been recognized in the pertinent art of Biever. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Biever by forming voids in the substrate as taught by Doyle et al. to reduce current leakage (col. 1, lines 55-59).

Referring to claims 12 and 18, Doyle et al. disclose the substrate as silicon (col. 3, lines 27-53).

Referring to claims 19 and 20, Doyle et al. disclose the predetermined strain is approximately 4% (col. 3, lines 39-44).

Claims 23-25, 30, 34, 42, 45, 47, 48, 50, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al. in view of Belford.

Doyle et al. disclose the subject matter claimed above expect performing a bond cut process.

Referring to claims 34 and 46, Belford discloses a method for forming a wafer where a central region of a substrate wafer (206) is flexed; performing a bond cut (smart

cut) process to form a silicon membrane from a crystalline sacrificial wafer, bonding a peripheral region of the substrate wafer (206) to a peripheral region of a silicon membrane (202) when the substrate wafer (206) is in the flexed position; relaxing the substrate wafer (206) to induce a predetermined strain in the silicon membrane (Fig. 2; col. 3, lines 18-33 & 63-67).

Since Doyle et al. and Belford are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Belford would have been recognized in the pertinent art of Doyle et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Doyle et al. by performing a bond cut process as taught by Belford to reduce the short channel effects (col. 1, lines 45-63).

Referring to claims 23-25, Dolye et al. disclose the predetermined strain is approximately 4% (col. 3, lines 39-44).

Referring to claims 30 and 42, Doyle et al. disclose implanting helium ions into the sacrificial wafer to form cavities along a cleavage plane; and heat-treating the sacrificial wafer and the substrate wafer combines cavities along the cleavage plane such that the sacrificial wafer is separated from the silicon membrane along the cleavage plane (col. 3, line 64 thru col. 4, line 22).

Referring to claims 45 and 48, Belford discloses wherein the semiconductor layer is wafer-sized (Fig. 1 & 2;col. 3, lines 6-33).

Referring to claims 47, and 51-53, Doyle et al. disclose the subject matter claimed above including forming a gate separated from the strained semiconductor

layer by a gate insulator; and forming first and second diffusion regions separated by a channel region, the strained semiconductor layer including the first and second diffusion region and the channel region (Fig. 2A & 2B; col. 3, lines 27-43).

Referring to claim 49, Belford discloses applying a pressure to flex the substrate wafer to have a predetermined strain includes applying a pressure to a substrate wafer having a thickness sufficiently small such that the substrate wafer is flexible (col. 3, lines 6-32).

Referring to claim 50, Belford discloses bonding the upon bonding the semiconductor membrane and the substrate wafer form a composite structure, the method further comprising bonding the composite structure to a carrier substrate (204) (col. 3, lines 16-33).

Claims 29, 39, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belford in view of Yamazaki et al. (6,902,616).

Belford discloses the subject matter above except forming a convex contour in a surface of a sacrificial crystalline wafer.

Referring to claim 39, Yamazaki et al. disclose a method for forming a wafer where including a convex contour in a surface of a sacrificial crystalline wafer; and bond a ultra-thin semiconductor membrane to a substrate wafer, wherein the ultra-thin semiconductor membrane is flattened and strained when bonded to the substrate wafer (col. 5, lines 46-61).

Since Belford and Yamazaki et al. are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Yamazaki et al. would have been recognized in the pertinent art of Belford. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Belford by forming a convex contour in a surface of a sacrificial crystalline wafer as taught by Yamazaki et al. to increase threshold voltage (col. 2, lines 8-34).

Referring to claims 29 and 41, Yamazaki et al. disclose heat-treating the sacrificial wafer and the substrate wafer; and separating the sacrificial wafer from the membrane such that the silicon membrane remains strongly bonded to the substrate wafer (col. 3, lines 30-34).

Referring to claim 40, Belford discloses the semiconductor membrane includes an ultra-thin semiconductor layer (col. 3, lines 16-33).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Zandra V. Smith
Supervisory Patent Examiner
20 March 2006